Design of a Low Power UWB Integrated Circuit for Endoscope Applications

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ABSTRACT

This paper presents the integrated circuit design of an ultra-wideband (UWB) transceiver for a wireless endoscope that enables real-time diagnosis with high resolution images. The implemented UWB transceiver is a non-coherent transmit reference (TR) architecture with differential binary phase shift Keying (DBPSK) modulation. All-digital pulse generator (PG) and merged radio frequency (RF) front end including low-noise amplifier (LNA), mixer and low-pass filter (LPF) have been proposed and implemented along with the analog baseband and LC-voltage controlled oscillator (VCO) using 0.18μm digital CMOS process.

1. INTRODUCTION

The advances in CMOS and micro-electro-mechanical Systems (MEMS) has caused radical changes in in vivo biomedical devices. As a result, wide varieties of implantable medical devices (IMDs) are currently being used in diagnostic, surgical and therapeutic purposes. However, the performance of current wireless communication link in IMDs falls much short for applications where high data rate and real-time link are mandated. Ultra-wideband (UWB) has gaining popularity as a promising technology in wireless personal area networks (WPANs) and wireless body area network (WBAN) due to the benefits from the impulse transmission nature of a digital baseband. So its deployment in the medical applications are highly desirable, as there are potential advantages such as higher data rates, lower power dissipation and enhanced security of medical data due to low equivalent isotropic radiated power (EIRP) limit, which results in low probability of interception and detection. In this paper, for the first time we deploy UWB technology in the biotelemetry system. In this paper we propose an UWB system for next generation biotelemetry systems, characterized by high data rate, low area, low power dissipation, and multi-channel bi-directional communication to allow link for real-time diagnosis.

*The required data rate is 110Mbps for high resolution images: (640×480 (pixels)×8(bpp)×3(RGB)×15(fps)=110Mbps)*

2. SYSTEM OVERVIEW

A conventional wireless endoscope system shown in Fig. 1 is comprised of a capsule endoscope for image capturing, an external unit for data recoding, analysis and diagnosis of syndrome in the gastrointestinal tract. The capsule endoscope is compose of a miniaturized camera, light-emitting diodes, CMOS imager, system controller, image processor, radio transceiver and battery. However, the current state-of-the-art systems suffer from the image distortion due to low resolution limited to a maximum of about 90,000 pixels, maximum of up to 14 image frames per second, and limited to total of 2,600 images, resulting in unintentional oversight of important spots with abnormalities [1–3]. They also suffer from serious control problems from the unidirectional transmission.

Our proposed endoscope system is similar to conventional systems, with one notable differences; omission of the image compression unit, as we take the advantage of high data transmission afforded by the proposed UWB transceivers, and
the deployment of the state-of-the-art multiple antenna technology (not discussed in this paper) in the external unit to dramatically improve the received signal to noise (SNR). The minimum data rate of 125Mbps in the proposed system is more than enough to transmit high resolution raw uncompressed image data (image frame size with minimum resolution of 640×480 = 307,200 pixels). The ability to transmit images in raw format in real-time removes the need for the image processor in the capsule, thereby reducing silicon area and power dissipation.

A non-coherent transmitted reference (TR) UWB architecture with differential binary phase shift keying (DBPSK) modulation was selected as the best option, based on the system simulations \cite{4} using the IEEE 802.15.4a channel model. The frequency bandwidth is at the lower UWB band (3.1~5.1GHz). This paper focuses on the implementation of UWB transceiver in the endoscope capsule shown in Fig. 1(b).

![Fig. 2. 15pJ/pulse All-Digital UWB Pulse Generator with Pulse Shape, Amplitude and Tx power Tuning Capacity](image)

![Fig. 3. An All-Digital PG: (a) Fine delay element, (b) Coarse delay element, (c) Bias basing circuit for the control of DEs, (d) Control signals for the H-Bridge and generated pulses](image)

![Fig. 4. Tx simulation: (a) Waveforms generated from the PG, (b) Power controllability of the Gaussian pulses, (c) PSD of the generated 5th derivate Gaussian pulse fully in compliance with FCC mask](image)

### 3. TRANSMITTER ARCHITECTURE

#### A. All-digital Pulse Generator

The proposed novel all-digital UWB Pulse Generator (PG) with pulse tuning capability (pulse shape, amplitude and transmit power) is show in Fig. 2. The proposed PG has ultra low dynamic energy consumption of 15pJ per pulse and no static current flow at the maximum of 200MHz pulse repetition frequency (PRF). Due to implantable nature of the device, there multiple constraints for the design of PG. They include limit on area, power dissipation from the low capacity battery, and severe attenuation through the human tissue (30~40dB in the GHz band) requiring controllable transmit power to combat its effects. The PG in Fig. 2 consists of
minimum sized digital PG gates, current starved coarse and fine grain delay elements (DEs) and the H-bridge output stage. The first stage of the circuit differentiates between the “1” and “0” data bits, respectively thorough $\text{pos\_sig}$ and $\text{neg\_sig}$ signals in order to generate bi-phase pulses. Two parallel NAND gates generate very short high-to-low pulses ($\text{pulse}$, $\text{d\_pulse}$). The pulse width and the relative delay between the short pulses are controlled by the fine delay element ($\text{FDE}$) and the coarse delay elements ($\text{CDE1}$, $\text{CDE2}$) (Fig. 3(a)-(c)). The DEs determine the pulse width and phase at the H-bridge output. MUXs select between the pulse and its delayed version depending on the value of the input datum. The generated pulse and its delayed version in turn generate two sets of high-to-low and complementary low-to-high pulses to control the cross coupled PMOS and NMOS pairs in the H-bridge (Fig. 3d). The $\text{P1}$ and $\text{N1}$ pair is turned on simultaneously by $\text{H2L\_1}$ and $\text{L2H\_1}$ signals (generated by $\text{CDE2s}$). The other pair $\text{P2}$ and $\text{N2}$ is turned on with a timing offset controlled by $\text{CDE1s}$. Bi-phase pulse at the output of the H-bridge is generated by changing the relative order of the control signals for each cross coupled P/NMOS pairs. Several versions of H-bridge output signals are shown in Fig. 3(d). The proposed PG circuit is remarkably simple when compared with other circuits with similar functionalities [5]. Table I tabulated the bias condition of the DEs and along with the pulse characteristics. As seen the transmit power delivered to a load of 50$\Omega$ for the 5th derivative Gaussian pulse, ranges from 29 to 71uW. The 5th derivative pulse can satisfy the FCC spectral mask without any extra circuitry [6] such bandpass filter, passive components and energy consuming power amplifier. As a result, the proposed PG achieves low area ($90 \times 50 \mu m^2$), low power consumption (2.8mW@200MHz PRF at 1.5V power supply), and it is fully compliant with the FCC mask, achieving all with a simple digital circuit described.

The PG simulation results are shown in Fig. 4. The Gaussian, its 1st and 5th derivatives pulses are shown in Fig. 4(a). Fig 4(b) shows the transmitted power controllability feature of the proposed PG using the DEs. The power spectral density (PSD) and its full compliance with FCC mask are illustrated in Fig. 4(c). Fig. 5 shows the layout implementation of the PG.

B. Voltage-controlled Oscillator

The use of impulse-UWB signaling implies tight timing tolerances. So the current-reuse CMOS differential LC-voltage controlled oscillator (VCO) with low phase noise and wide tuning range [7] (Fig. 6) is used in preference to a ring oscillator. In this VCO, negative conductance is provided by the cross connected P/NMOS transistor pair to compensate for the losses in the LC-tank. The cross coupled P/NMOS configuration reduces the supply current by half compared with the conventional LC-VCO, while providing the same negative conductance. The centre frequency tuning range
extends the desired 3.1G~5.1GHz bandwidth, with low phase noise of –100dBc/Hz at 100kHz offset. The power consumption for the VCO is 1.2mW at 400MHz center frequency, at 1.5V power supply.

4. RECEIVER ARCHITECTURE

A. Wideband Merged LNA, Mixer and LPF

We propose a novel wideband RF front end, where low noise amplifier (LNA), mixer and low pass filter (LPF) circuits are merged as illustrated in Fig. 7. Wideband LNA is the most challenging block in the UWB system design with low power constraint as it has to provide sufficient gain and wideband input matching to amplify the UWB signal over wide bandwidth with minimum noise figure (NF). The concept of the stacked LNA and mixer was introduced in [8]. Shortening the signal paths (stacked connection), by reducing the number of transistors and removing the passive components for the power matching, achieves a lower current consumption, higher linearity and lower NF. The broadband input matching was attained through the use of a cascode LNA with a bandpass response. LC high pass filter (HPF) of C1 and L1 achieves the lower frequency input matching at 3.1GHz. The input matching at the higher frequency of 6.5 GHz is obtained through inherent LPF response characteristic of cascode LNA [9]. Passive mixer is an attractive design choice in the direct conversion receiver (DCR) with a low power constraint as it dissipates no DC current and provides high linearity. The absence of the DC current in the switches removes the 1/f noise that is most troublesome in the DCR. The stacked 1st order LPF (Rt and Ct) further reduces the signal path, thus improving linearity and NF.

Fig. 8 shows the simulated S-parameters and NF performance for the single stage common source (CS) cascode LNA part of Fig. 7, with the output buffer added for output matching purpose. As seen S21 is 11dB, S11 is less than –10dB, NF is around 3dB in the entire frequency bandwidth (3.1~5.1GHz). P1dB and IIP3 are –13dB and –3dB, respectively. It draws 5mA at 1.5V power supply.

The simulation results for the merged RF front end, when the Local Oscillator (LO) power is 0~5dB are shown in Fig. 9. On the other hand, in designed merged RF front end, the achievable S21 is 16dB, S11 is less then –10dB, and NF is around 8dB. P1dB and IIP3 are –11dB and 0.3dB, respectively. It only consumes 3.5mA. The values obtained for S21, P1dB and IIP3 parameters are 11 dB, 2 dB and 2.7dB better than their corresponding values for the conventional cascaded configuration of LNA, mixer and LPF. The 16dB conversion gain (S21) of the merged RF front is obtained even with the passive mixer having a conversion loss.

The current consumption of the merged RF front end is even 1.5mA smaller than the standalone LNA. Moreover, in response to an intermittent signal the merged RF front end can be placed in power save mode through the synchronized bias switching enable signal (ctl_En) connected to the common gate (CG) transistor. While the bias is turned off the no current flows through the circuit, significantly improving the energy efficiency, as the merged RF front end circuit takes the largest portion of power consumption in the receiver.

![Fig. 10. Analog baseband receiver circuit](image-url)
B. Analog Baseband

The baseband circuit comprising of an integrator, negative feedback amplifier and comparator is shown in Fig. 10 [10]. The operational transconductance amplifier (OTA) is used as the integrator that converts differential input signal to single-ended output signal. The output voltage of the merged RF front end is applied to the input terminals of the integrator. The negative feedback amplifier biases the integrator output. The final stage is a two stage comparator. The P/NMOS transistors switch between on and off positions depending on the applied signal. The final stage obtains the output base band signal corresponding to the transmitted PRF. The analog baseband dissipates 87µW of power.

The simulation results for the integrated UWB receiver for –40dB, 4.1 GHz input signal, 200MHz base band signal, and 3.9 GHz VCO, is shown in Fig. 11. The overall performance of the UWB transceiver is summarized and compared with work in [2] in Table II. We achieve a data rate 123 times higher than the work in [2] with a energy per bit that is lower by 3 orders of magnitude.

5. CONCLUSION

The proposed UWB transceiver for wireless endoscope was presented and implemented in 0.18µm digital CMOS process. The proposed novel low power all-digital UWB PG with pulse tuning capability is a suitable candidates for the UWB data communication where high PRF with low area and power dissipation are required. The controllable transmit power is a useful mean to fight the severe tissue attenuation. The stacked merged RF front end including LNA with the bias switch, mixer and LPF exhibits low power dissipation, low NF and higher linearity, achieved by removing the noisy signal paths and the power efficiency is better than that of the single CS cascade LNA. Our proposed design achieves an impressive data rate of 125Mbps at ultra low 15pJ/bit transmit energy.

REFERENCES


![Fig. 11. The simulation results for the UWB receiver (a) analog baseband integrator output, (b) the comparator intermediate output, (c) the comparator final output.](image-url)