Memristor Pattern Recognition Circuit Architecture for Robotics

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ABSTRACT

Pattern recognition solutions based on software are often limited by the speed of data transfer between memory and processor circuitry. Solutions based on application specific electronic hardware can be faster but are limited in adaptability to new patterns. These deficiencies in pattern recognition present a hurdle in further developing new applications in robotics. Last year researchers at HP Labs noted a connection between hysteretic resistance behaviors of some thin film oxides with a theoretical circuit element called a "memristor," originally predicted in 1971 and possessing both data storage and signal processing capabilities. The present article describes the memristor and presents an example of a memristor pattern recognition circuit architecture combining the optimum characteristics of software and hardware pattern recognition solutions.

Keywords: Memristor, Pattern Recognition, Robotics, RRAM, Crossbar

1. INTRODUCTION

In 1971, Prof. Leon Chua of UC Berkeley published a paper [1] arguing that the conventional view of passive circuitry consisting of resistors, capacitors, and inductors was incomplete. A new fundamental circuit element called the "memristor" (memory resistor) was proposed as a fourth fundamental circuit element based on a relationship between the time integral of voltage and charge. A subsequent paper [2] in 1976 by Chua and Sung-Mo Kang extended and formalized the theory to cover a broader range of systems characterized by a pinched hysteresis curve (Fig. 1). Under a sufficiently small voltage the curve demonstrates the linear behavior between current and voltage characteristic of resistors but as the voltage is increased the slope of the curve switches resulting in a different resistance state. Another characteristic property noted in the 1976 paper was frequency dependence such that the pinched hysteretic curve degenerated into a typical linear resistor at high frequencies. The initial papers of Chua and Kang represented a theoretical foundation for the memristor, but at the time was no apparent physical implementation to enable integration of memristors in electronic design. This situation changed as of last year when a paper [3] from researchers at HP Labs identified a similarity between the memristor model and the behavior of ionic switching systems formed from thin film oxides. A pinched loop hysteretic curve based on Pt-TiO_{2-x}-Pt was found to be identical to that of a memristive system with similar frequency degeneration. But while HP's group was the first to recognize the connection between the hysteretic property of some thin film oxides and the memristor theory they were not the first to identify the hysteretic effects of thin oxides in and of itself. As early as 1967 [4] researchers have identified hysteretic properties of thin film oxides but have lacked a cohesive explanation for the effect. In the past decade this research has accelerated due to the desirability of a new form of higher density non-volatile memory called Resistive Random Access Memory (RRAM) [5, 6].

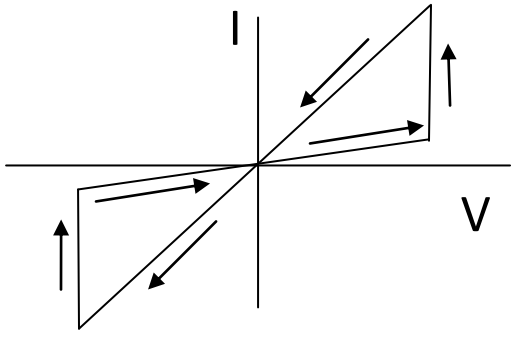

Fig. 1 Illustrative example of a typical hysteretic I-V characteristic of thin film oxide memristive materials.

However, non-volatile memory is not the only proposed application for these devices. With both a theoretical foundation and material examples of memristors in place numerous potential applications of memristive systems to self-repairing circuitry [7], analog arithmetic processing [8], signal processing [9], neuromorphic systems [10], and analog control systems [11] have already been proposed. Many of these applications will undoubtedly have an impact to robotic systems but one application particularly critical to robotics is pattern recognition. The following sections further detail the memristors as components of crossbar arrays, a circuit model for memristive junctions, and a memristor pattern recognition circuit architecture applicable to robotic design.

2. MEMRISTOR CROSSBAR DESIGN AND MODELING

Since the late 1990's crossbar arrays have been proposed as a candidate platform for future nanoelectronics circuit architectures combining the advantages of high density with reconfigurability [12] (Fig.2a). However, depending on the material use as the bistable junction, a noted deficiency in crossbar arrays is internal feedback paths between junctions of the crossbar array [13]. Solutions to this problem include the fabrication of a pn junction layer or Schottky junction between wiring and the bistable switching junction (Fig. 2b) [11].

By providing memristors as the bistable junction, a model may be developed for the crossbar transfer function based on Ohm's Law. For an input voltage V_i applied to the i^{th} column wire (with the row wires grounded), the current flow through the memristance material at the intersection of the i^{th} column and j^{th} row is given by :

$$I_{ij} = \frac{(V_i - V_{DIODE})}{R_{ij}(w)} \qquad Eq.(1)$$

where V_{DIODE} is the diode threshold and $R_{ij}(w)$ is the resistance associated with the memristor dependent upon state variable w. The value of w is associated with the amount of ionic drift in the memristive material and is dependent upon the history of the voltage applied to the memristor. Based on Kirchhoff's Current Law the total current transferred to each row of the crossbar is:

$$I_j = \sum_i I_{ij} = \sum_i \frac{(V_i - V_{DIODE})}{R_{ij}(w)} \qquad Eq.(2)$$

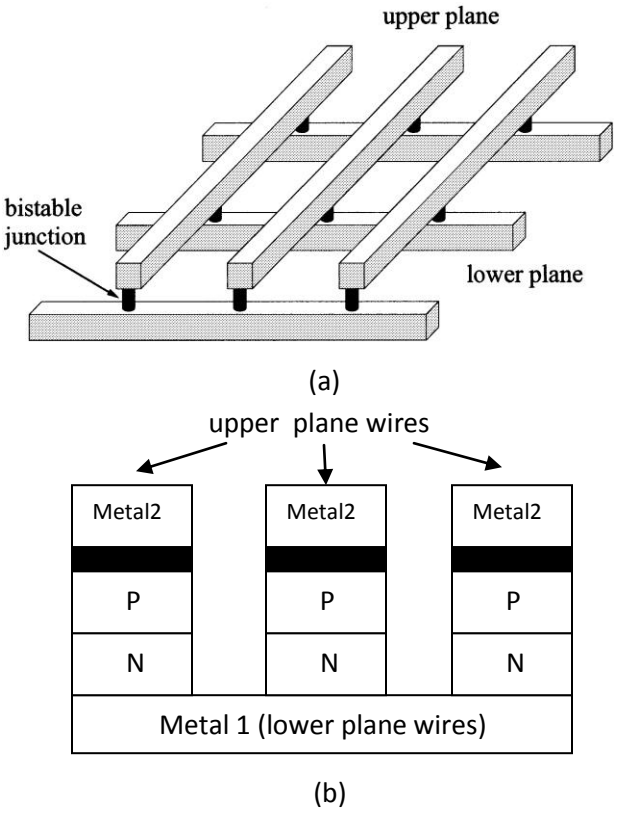

Fig. 2 (a) Crossbar array (b) Cross-section of crossbar array incorporating pn junction layer fabricated in series with the bistable junction.

Experimental pinched hysteresis I-V curves [3,5,13] indicate a region of applied voltage over which the memristance variation can be approximated by a resistor having one of two possible values (R_{OFF}, R_{ON}) dependent on the applied voltage history with ratios of R_{OFF} to R_{ON} being 10^6 or greater for some materials. The frequency dependent behavior is also indicative of a parallel capacitance (C_p) in which the pinched hysteresis curve degenerates to a singular resistance (R_s) independent of the history of the applied voltage. These combined effects lead to an approximate circuit model for a memristor junction as indicated by Fig. 3 in which the position of switch S1 is dependent on the voltage states previously applied to the junction. It is noted that for some materials a switching effect may also be associated with the capacitance in addition to the resistance as described in [14] and theoretically investigated in [15]. A more detailed mathematical model is described in [16] including both resistive and capacitive hysteretic switching mechanisms based on a thin film nanoionic material.

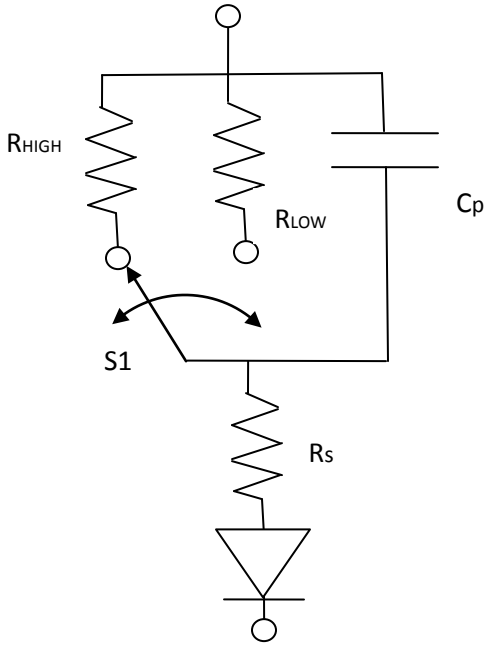

Fig. 3 Approximate small signal circuit model for memristor crossbar junction

3. PATTERN RECOGNITION CIRCUIT ARCHITECTURE

Some generally desirable goals for pattern recognition circuitry are the following:

1. Robustness/invariance to variations of the input pattern.
2. Adaptability of circuit to identify new recurrent patterns.
3. Speed of responsiveness to pattern inputs.

The first and second of these goals are achievable with software using a sufficiently large memory storing a large number of patterns in a look up table. However, a lag in responsiveness increases in accordance with the number of stored patterns in memory. Application specific electronic hardware may meet the goal of speed of responsiveness but only for a limited number of patterns sacrificing adaptability. Memristors offer the possibility of a hybrid approach by placing a memristor crossbar array directly in a control signal flow path. The binary resistance states can thus serve both the functions of data storage and signal processing.

One approach to pattern recognition using this capability of memristor crossbars would be to control a current output to be based upon bit matches between input signal states having high or low voltage values and reconfigurable memristance states having high or low resistance values. Fig. 4 illustrates an example of a circuit configuration performing such bit matching using a memristor crossbar array interconnecting digital and analog processing circuitry. Inverted resistance states for the memristors along with inverted voltage states for the input signals may be achieved using the inverter circuitry connected to the crossbar columns. Based on Eq. (2) and provided that $R_{OFF}>>R_{ON}$ the current transmitted from each row of the circuit of Fig. 4 is given by:

$$I_j = \sum_i \frac{(V_i - V_{DIODE})}{R_{ij}(w)} + \sum_i \frac{\overline{(V_i - V_{DIODE})}}{\overline{R_{ij}(w)}} \quad Eq.(3)$$

where the over line notations denote inverted voltage and memristance states. Based on the I-V curves of particular memristive materials, the resistance states associated with the memristances M_{ij} are constant for an applied voltage less than a certain threshold value V_{DIODE}. From Eq. 4 the output current from each crossbar junction is near zero if the voltage logic state is different than the memristive logic state while identical logic states result in a current of approximately V_{HIGH}/R_{ON}. The following table summarizes the possible combinations of voltages and memristance states for a single bit matching combination.

TABLE 1 : Binary voltage/memristance comparison states

V_i ($<V_{DIODE}$)	M_{ij}	I_j
$V_{LOW} < V_{DIODE}$ (logic 0)	R_{OFF} (logic 0)	$\approx V_{HIGH}/R_{ON}$
$V_{LOW} < V_{DIODE}$ (logic 0)	R_{ON} (logic 1)	≈ 0
$V_{HIGH} > V_{DIODE}$ (logic 1)	R_{OFF} (logic 0)	≈ 0
$V_{HIGH} > V_{DIODE}$ (logic 1)	R_{ON} (logic 1)	$\approx V_{HIGH}/R_{ON}$

For n bit matches between a particular voltage bit patterns and the memristance bit patterns of a particular row the output current is thus:

$$I_j = \frac{nV_{HIGH}}{R_{ON}} \quad Eq.(4)$$

By setting the current level detection circuitry of Fig. 4 to a threshold determined by Eq. 4 with n=3 the relationship between the motor actuation signals and the sensor logic levels is given by TABLE 2.

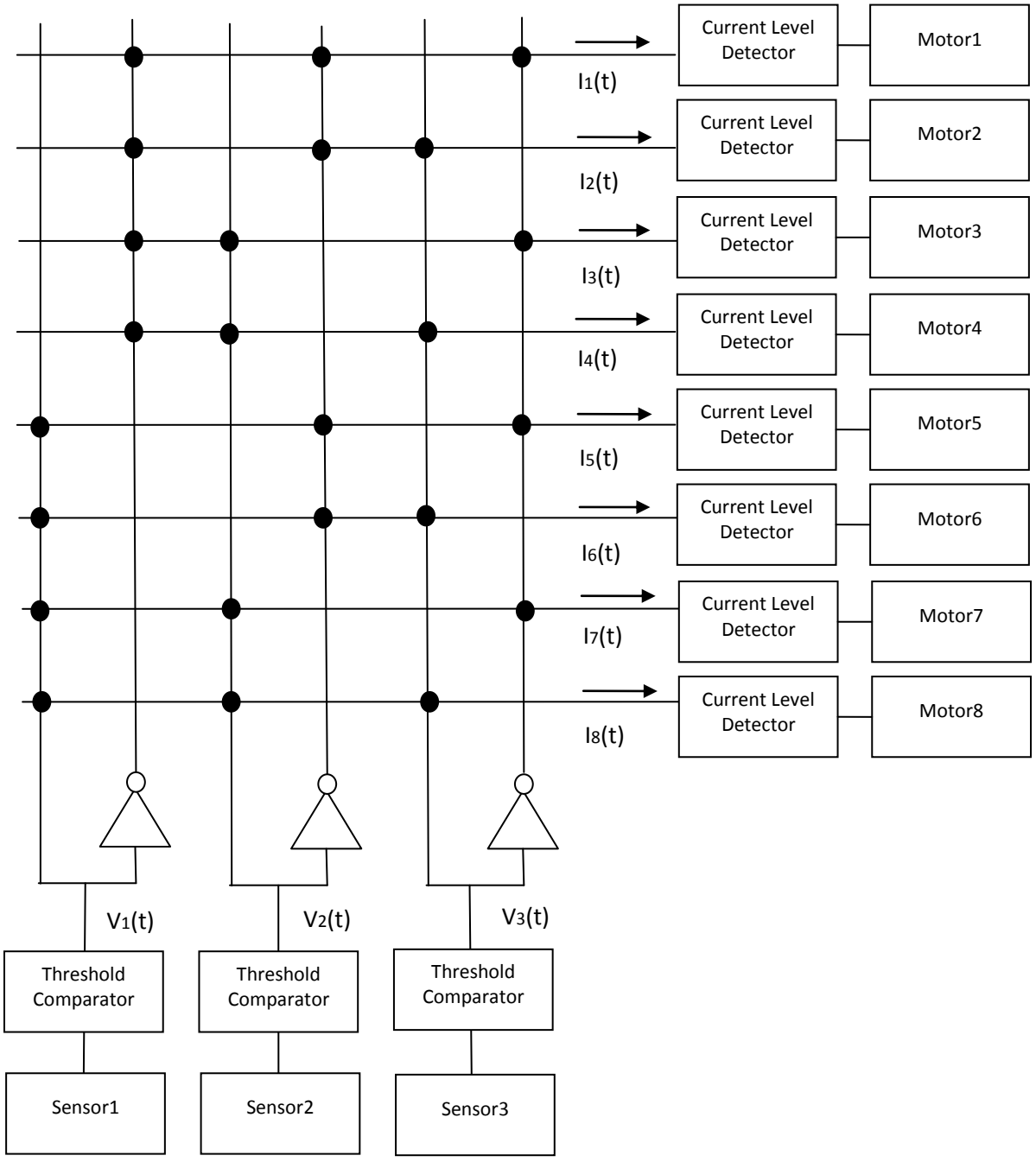

Fig. 4 Pattern recognition circuit for robotics using 3x8 memristor crossbar configuration placed in the signal flow path between an array of sensors and an array of motors. Low resistance memristances states are represented by black dots.

TABLE 2 : Motor control as a function of actuated sensors

Sensor 1	Sensor 2	Sensor 3	Motor Actuated
0	0	0	Motor 1
0	0	1	Motor 2
0	1	0	Motor 3
0	1	1	Motor 4
1	0	0	Motor 5
1	0	1	Motor 6
1	1	0	Motor 7
1	1	1	Motor 8

In this example the functional correspondence between sensor signals and actuator signals acts as a decoder, but due to the reconfigurable nature of memristive materials the decoder transfer function can be changed providing adaptability in the motor/sensor responses. Controlling the voltage levels via the threshold comparators can switch the control circuit between a learning mode, in which the memristive resistance states of the crossbar array are written to performing a memory function or to a processing mode below the threshold of memristive switching in which the resistance states serve as a logic or processing function as in TABLE 2. In addition, for larger input bit patterns flexibility can be provided in the number of bits matches required for a motor actuation signal by adjusting the threshold of the current detectors. In such a case, a digitalized vocal pattern or image including a great deal of corruption could still produce an actuation signal.

5. CONCLUSIONS

While the circuit of Fig. 4 is only a simple example of the potential that memristor crossbar circuitry offer for pattern recognition there is no clear roadblock to scaling up such a system to accommodate larger sensors arrays having hundreds or thousands of sensor inputs and hundreds or thousands of actuator elements. Since the binary resistive states of the memristor crossbar junctions essentially function as a reconfigurable bit pattern array they serve the function of data storage. Since the memristor crossbar junctions are also directly within the control signal flow path and set up a decoding transfer function between sensed input and actuator outputs they perform the function of data processing. Integration of data storage and data processing in a single circuit has the potential to overcome the bottleneck caused by the data retrieval times from increasingly larger memories. In addition, since the memristor crossbar states essentially function as software the potential exists for combining evolutionary computing techniques conventionally limited to software such as hill climbing and genetic algorithms to electronic hardware learning systems and produce more adaptive and responsive robotic systems.

6. REFERENCES

[1] L.O. Chua, "Memristor-The Missing Circuit Element," **IEEE Transactions on Circuit Theory**, Vol. 18, No. 5, September 1971, pp. 507-519

[2] L.O Chua, S.M. Kang, "Memristive Devices and Systems," **Proceedings of the IEEE**, Vol. 64, No. 2, February 1976, pp.209-223

[3] D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, "The missing memristor found," **Nature**, Vol. 453, May 2008, pp. 80-83

[4] J.G Simmons, R.R. Verderber, "New conduction and reversible memory phenomena in thin insulating films," **Proceedings of the Royal Society of London A**, 301, 1967, pgs. 77-102

[5] S.Q Liu, N.J. Wu, A. Ignatiev, "Electric-pulse-induced reversible resistance change effect in magnetoresistive films," **Applied Physics Letters**, Vol. 76, Issue 19, May 2000

[6] A. Beck, J.G. Bednorz, C. Gerber, C. Rossel, D. Widmer, "Reproducible switching effect in thin oxide films for memory applications," **Applied Physics Letters**, Vol. 77, Issue 1, July 2000

[7] G.S. Snider, "Self-organized computation with unreliable, memristive nanodevices," **Nanotechnology**, Issue 36, August 2007

[8] B.Mouttet, "Logicless Computational Architectures with Nanoscale Crossbar Arrays," **NSTI Conference**, June 1-5, 2008

[9] B.Mouttet, "Proposal for Memristors in Signal Processing," **Nano-Net Conference**, Sept. 14-16, 2008

[10] G.S. Snider, "Memristors as Synapses in a Neural Computing Architecture," **Memristor and Memristive Systems Symposium**, November 21, 2008

[11] B.Mouttet, "Proposals for Memristor Crossbar Design and Applications," **Memristor and Memristive Systems Symposium**, November 21, 2008

[12] J.R. Heath, P. J. Kuekes, G.S. Snider, R.S. Williams, "A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology," **Science**, Vol. 280, June 12, 1998

[13] M. Liu, W. Guan, S. Long, Q. Liu, W. Wang, "Excellent Resistive Switching Characteristics of Cu-doped ZrO2 and its 64 bit Cross-point integration," **The 9th International Conference on Solid-State and Integrated-Circuit Technology**, October 20-23, 2008.

[14] S.Tsui, A.Baikalov, J.Cmaidalka, Y.Y. Sun, Y.Q. Wang, Y.Y. Xue, C.W. Chu, L.Chen, A.J. Jacobson, "Field-Induced Resistive Switching in Metal-Oxide Interfaces," **Applied Physics Letters**, February 27, 2004.

[15] M.D. Ventra, Y.V. Pershin, L.O. Chua, "Circuit elements with memory: memristors, memcapacitors, and meminductors," **arvix.org cond-mat**, January 23, 2009

[16] B.Mouttet, "An Introduction to Memimpedance and Memadmittance Systems Analysis," **Google Knol**, February 01, 2009