ABSTRACT

WiMAX (Worldwide Interoperability for Microwave Access) is one of the standards for high-speed wireless communications. The development cycle of a WiMAX processor is short because a transmission rate of a WiMAX system improves gradually. To keep using it even when the speed improves, there is a method of development that uses a processor that can be a reconfiguration of circuits. In this paper, a mobile WiMAX processor by using a CPLD (Complex Programmable Logic Device) is proposed. Because wave-pipeline technique is used, the problem of processing speed is canceled. The authors evaluate wave-pipelined circuits which WiMAX processor needs on a CPLD. It is made clear that wave-pipeline technique is effective in the circuits on the CPLD.

Keywords: WiMAX, CPLD, FPGA, wave-pipelining, gate-level simulation.

1. INTRODUCTION

WiMAX[1] (Worldwide Interoperability for Microwave Access) which is based on IEEE 802.16 standard is a standard for high-speed wireless communications. It can be used as an alternative to FTTH (Fiber To The Home), cable and DSL (Digital Subscriber Line) in a region where they cannot be used. The use of a WiMAX system makes that the high-speed Internet can be used in various regions. It solves social various problems which are a health disparity and an education gap, etc.

In general, a processor for a wireless data communications system is a system LSI by customizing. Development of the system LSI has a problem in the point of a development cycle. Because a transmission rate of a WiMAX system improves gradually, the development cycle is short. That is, it is a cause of a high cost.

The full speed of a mobile WiMAX system which is based on IEEE 802.16e standard being served in Japan now is 40Mbps. Because the full speed on the standard is 75Mbps, the full speed of the system will be 75Mbps. When the service of 75 Mbps is started, the hardware for the mobile WiMAX used in Japanese cannot be used at 75 Mbps.

To keep using it even when the speed improves, there is a method of development that uses a processor that can be a reconfiguration of circuits. Its main current is a FPGA (Field Programmable Gate Array) and a CPLD (Complex Programmable Logic Device). The operation of the FPGA is more high-speed than that of the CPLD. Circuits on a lot of FPGAs stored in SRAM (Static Random Access Memory) cells. That is, when a power supply of a system which equipped with the FPGA turned on, circuits are loaded from SRAM cells.

Therefore, a power supply control of an entire WiMAX processor that used the FPGA is a cause of power consumption. Because a mobile WiMAX system is used with
a mobile computer that works with a battery, power consumption is important. Additionally, time to load circuits of the FPGA is consumed.

This paper is organized as follows. Section 2 presents outline of CPLD and FPGA and Section 3 presents outline of wave-pipeline technique. Then, Section 4 describe wave-pipelined circuits on CPLD for the WiMAX Processor. Wave-pipelined circuits are evaluated by gate-level simulations on Section 5. In section 6, the concluding remarks are made.

2. CPLD AND FPGA

A CPLD and a FPGA are a reconfigurable device, and circuits configurations of them are easily constructed by a circuits designer. Design of using the reconfigurable devices can be used for not only circuits evaluations but also systems development using feature of the reconfigurable devices [2]. Features of the CPLD and the FPGA are shown in Table 1.

<table>
<thead>
<tr>
<th>Device Type</th>
<th>CPLD</th>
<th>FPGA</th>
<th>Custom LSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programmable element</td>
<td>Flash, EEPROM</td>
<td>SRAM</td>
<td>Un-programmable</td>
</tr>
<tr>
<td>Operating speed</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
</tbody>
</table>

Circuits configurations of the CPLD are stored in a flash memory. The use of the flash memory is led to non-volatile circuits. On the other hand, circuits configurations of the FPGA are stored in a SRAM. It means that circuits of the FPGA are volatile. When we activate the FPGA, the circuits configurations must be loaded from a ROM. As a result, a frequent on/off of the power supply of the FPGA to reduce a power consumption is impossible.

However, the operating speed of the CPLD is slower than that of the FPGA and operable temperature range of the CPLD is narrower than that of the FPGA. Concrete temperature ranges are shown in Table 2 [3]. The CPLD demands a power-awareness design than the FPGA.

3. WAVE-PIPELINING

Not only high clock frequency but also low power dissipation can be obtained at the same time by wave-pipelining [4]-[6]. It exploits high throughput combinational logic blocks in which as many as data are launched unless they conflict. Although wave-pipelining was attempted to the entire region of a processor, it was viewed pessimistically because it requires removing general registers as well as pipeline registers from processors. It seems hard to eliminate general registers playing fundamental roles in sequential circuits. The insufficient power of CAD tools so far developed is another reason why wave-pipelines have been applied out of processors.

Accordingly, design and evaluation methods for wave-pipelines have not yet established well compared with those for conventional pipelines. Mostly wave-pipelines have been so far applied to simple unifunctional circuits such as adders, multipliers, counters, and DRAM. Regarding multifunctional wave-pipelines, a wave-pipelined ALU has recently appeared [7]-[10].

Then, a microprocessor developed by using wave-pipelines in part appeared [10]. It is 14-segment ULTRASPARC-III whose second and third instruction fetch segments have been wave-pipelined. Another example is an asynchronous wave-pipeline, though it is not compatible with conventional processors. Wave-pipelined CRC that is a sequential circuits has been developed by us [11].

The signal path of combinational circuit is uneven of delay time. The most high-speed signal in one group in a clock has the possibility to collide with the slow signal in just before clock. The problem was solved to wave-pipelined combinational circuit shown in Figure 1 (a) by the delay time of all signal paths is brought close at the delay time of critical path.

The relation between the clock cycle and delays is obtained as follows [6].
Here,

\[ T_{CK} > (D_{MAX} - D_{MIN}) + T_{OV} \]  \hspace{1cm} (1) \]

\( T_{CK} \): Clock cycle time

\( T_{OV} \): Overhead time

From Eq. (1), \( D_{MAX} - D_{MIN} \) should be close to 0 as much as possible in order to obtain minimum \( T_{ck} \). One of solution to satisfy this requirement can be conceived from Figure 2 that shows relation between time and logical depth.

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4. WAVE-PIPELINED CIRCUITS ON CPLD

A. CRC circuits

A CRC circuits include all circuits that multiplied return by shift register in some arithmetic circuits as shown in Figure 3 [10]. In the hardware of WiMAX, the CRC circuits are used. The physical layer starts by attaching CRC bits. These bits are used by the receiver to detect whether or not a transport block includes any errors after the channel decoding process.

![Figure 3 Conventional CRC Circuits.](image)

B. Wave-Pipelined CRC circuits for WiMAX

Table 3 shows development environment, and Figure 4 shows a logic circuit of wave-pipelined CRC circuits. Figure 4 (a) is CCITT and Figure 4 (b) is 32-bit CRC. Wave-pipeline technique should adjust delay time by the methods other than the use of a register. Here, we adjust delay time by using buffers. The use of a lot of registers is a cause of the increase of power consumption with a clock. Therefore, power consumption is increased in using it.

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<table>
<thead>
<tr>
<th>Function</th>
<th>Name</th>
<th>Vendor</th>
</tr>
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<tbody>
<tr>
<td>Microprocessor</td>
<td>Core 2 Duo</td>
<td>Intel</td>
</tr>
<tr>
<td>Main Memory</td>
<td>2.0 GHz 3 Gbytes</td>
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<td>Operationg System</td>
<td>Windows XP Professional</td>
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<td>Altera</td>
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<td>CPLD Device</td>
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<td>Altera</td>
</tr>
<tr>
<td>Power Estimator</td>
<td>MAX Power Calculator Spreadsheet Version 1.2</td>
<td>Altera</td>
</tr>
</tbody>
</table>
Figure 4 Wave-Pipelined CRC. (a) CCITT. (b) 32-bit CRC.

Figure 5 Gate-level simulation results of 32-bit wave-pipelined CRC circuits.
5. EVALUATION OF OPERATION CLOCK SPEED AND POWER CONSUMPTION

The authors have evaluated wave-pipelined CRC by using the development environment in Table I. Figure 5 shows the gate-level simulation result of 32-bit wave-pipelined CRC circuits. According to the result of gate-level simulation, it shows that the 32-bit wave-pipelined CRC circuits operate normally without using a register and by 111.1 MHz.

6. CONCLUDING REMARKS

In this paper, the authors proposed a mobile WiMAX processor by using a CPLD. The CRC circuits which WiMAX processor needs on a CPLD were evaluated. According to gate-level simulations, it was shown that operation speed of wave-pipelined CRC circuits on a CPLD is largely exceeds 75MHz. Power consumption which is important in a mobile data communications of wave-pipelined CRC circuits was evaluated. It is made clear that wave-pipeline technique is effective in the CRC circuits on the CPLD. The next step of our study is designing of wave-pipelined circuits in other parts of the WiMAX system.

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REFERENCES


